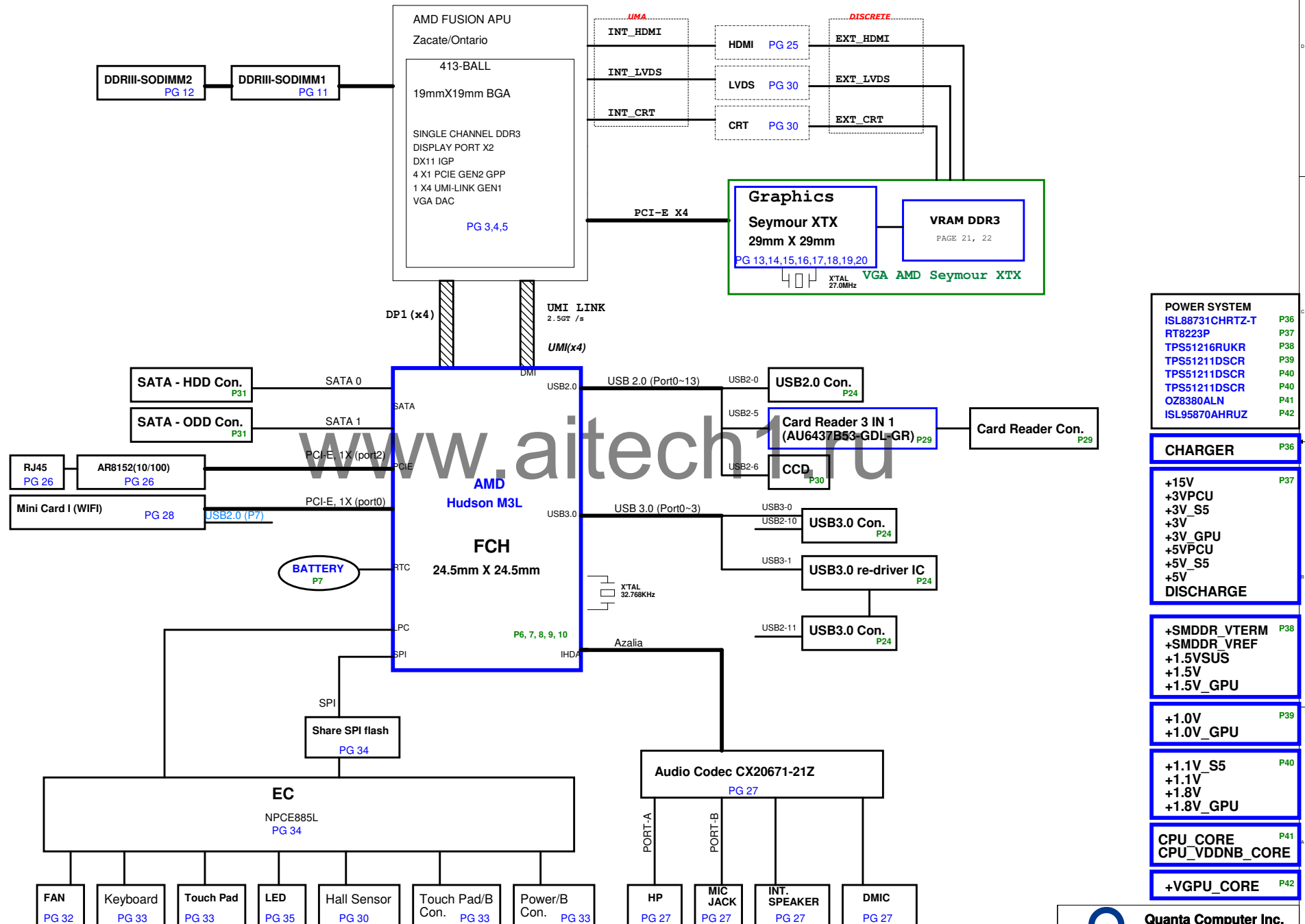


# 14" MTB/MTBD Brazos 2.0 Block Diagram

## PCB STACK UP






LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : SVCC  
LAYER 5 : IN2  
LAYER 6 : IN3  
LAYER 7 : GND  
LAYER 8 : BOT

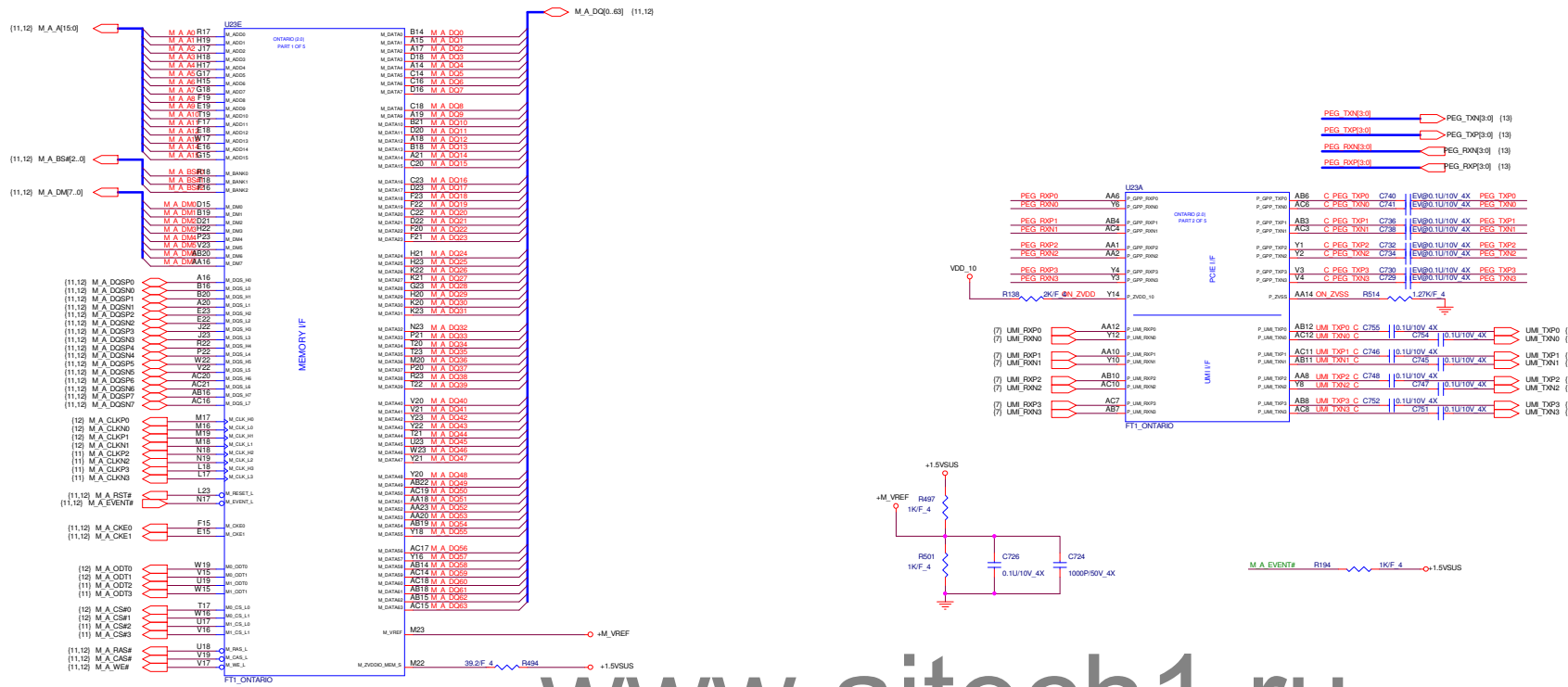


PAGE	DESCRIPTION	BOI FUNCTIONS
1	Schematic Block Diagram	
2	POWER STAGE & BOI-FUNCTION	
3 - 5	Processor	CPU
6 - 10	FCH	CLG
7	RTC	RTC
11 - 12	DDRIII SO-DIMM	DDR
13 - 20	Seymour XTX(M2)	VGA
21 - 22	VRAM - DDR3	VGA
23	RESERVE	VGA
24	USB Connector	USB
	USB 3.0 Redriver	U3B
	USB Sleep Charger	SLC
25	HDMI comm part	HDM
	CEC	CEC
26	Atheros LAN	LAN
27	Codec (CX20671-21Z)	ADO
28	MINI Card (Wi-Fi & WIMAX)	MNW
29	Card reader	MMC
30	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
31	HDD	HDD
	ODD	ODD
32	Thermal	THC
	FAN	THC
33	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
34	EC NPCE885LA0DX	KBC
35	LED	LED
36	CHARGER-ISL88731C	PWM
37	System 3V/5V(TPS51123A)	PWM
38	DDR 1.5V	PWM
39	+1.0V	PWM
40	+1.1V/+1.8V	PWM
41	CPU CORE	PWM
42	GPU	PWM
43	Power Tree	
44	Power Sequence	
45	Change List	

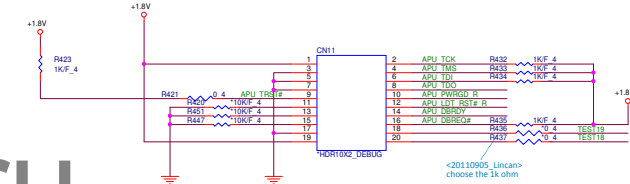
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAINON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAINON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.8V	+1.8V	MAINON	S0
+1.5VSUS	+1.5V	SUSON	S0~S3
+1.5V	+1.5V	MAINON	S0
+1.1V_S5	+1.1V	+1.1V_DUAL_EN	S0~S5
+1.1V	+1.1V	MAINON	S0
+1V	+1V	MAINON	S0
CPU_CORE	~	VRON	S0
CPU_VDDNB_CORE	~	VRON	S0
+VGPU_CORE		GPU_VRON	S0
+1.8V_GPU	+1.8V	GPU_MAINON	S0
+1V_GPU	+1V	GPU_PG_TV_EN	S0
+3V_GPU	+3.3V	GPU_MAINON	S0
+1.5V_GPU	+1.5V	GPU_MAINON	S0

ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	NMP@	LPC Debug Card
3	512M@	VRAM 512M
4	1GCA@	VRAM 1Gb*4(C-die, A-die)
5	1GEB@	VRAM 1Gb*4(E-die, B-die)
6	2G@	VRAM 2Gb
7	AMD@	AMD VRAM
8	Sam@	Samsung VRAM
9	EV@	DISCRETE
10	IV@	UMA
11	ECRT@	DISCRETE CRT
12	ICRT@	UMA CRT
13	EHM@	DISCRETE HDMI
14	IHM@	UMA HDMI
15	U3@	Internal USB 3.0
16	U2@	USB 2.0 (colay W USB 3.0)
17	ULD@	USB Port (Left Down)
18	ULU@	USB Port (Left Up)
19	ULU2@	USB 2.0 Port (Left Up)
20	ULU3@	USB 3.0 Port (Left Up)
21	UR@	USB Port (Right)
22	UR2@	USB 2.0 Port (Right)
23	UR3@	USB 300 Port (Right)

GND PLANE	PAGE
 8769GND	34
 GND	26
 GND	ALL
 ADOGND	27
 Shield_GND	27

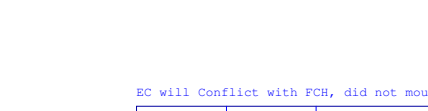


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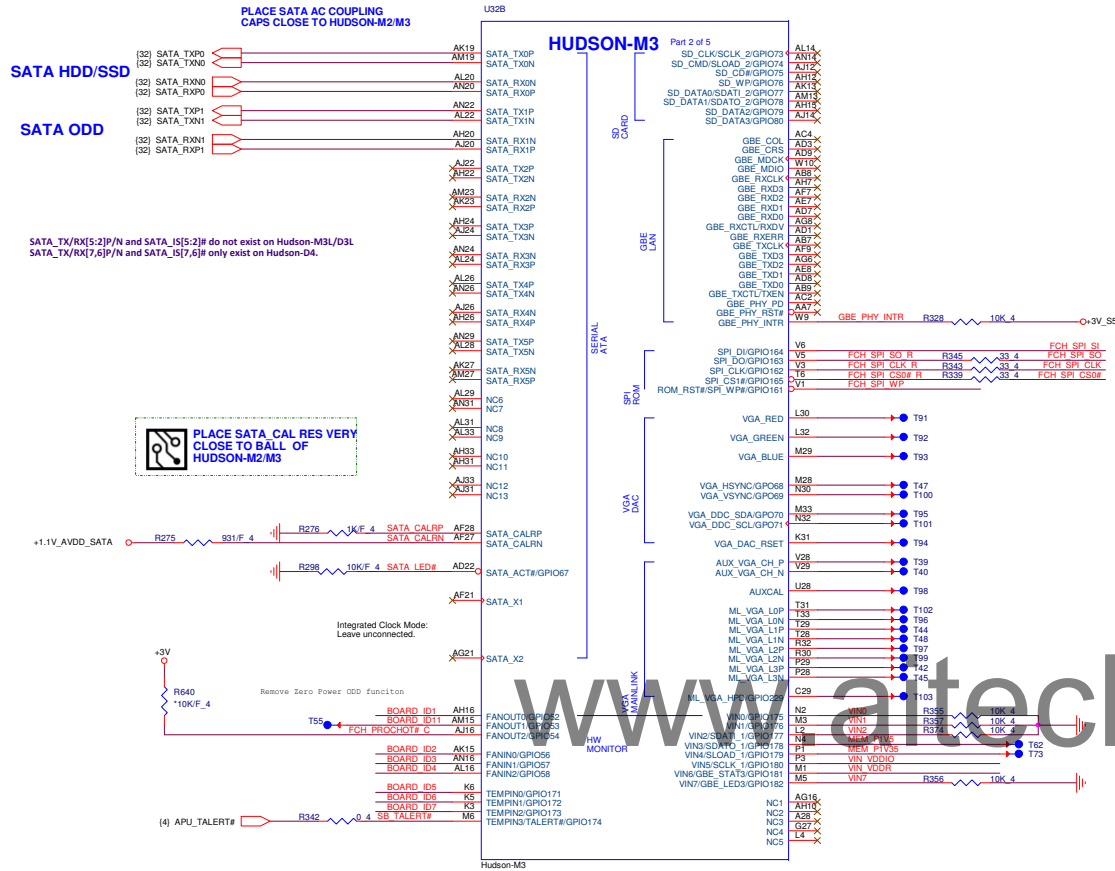
N,WLAN (27,29) FCH PCIE RST# 

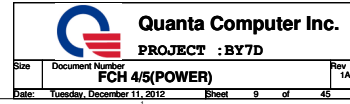


Date: Tuesday, December 11, 2012 Sheet 6 of 45

EC will Conflict with FCH, did not mount R315#R318					
EC	FCH	Device		I2C_Device(S)	
I2Ce_1 (M)	I2Cf_2 (M)	Charger	Battery		ALL/S5
I2Ce_2 (M)		EEPROM	APU		ALL
I2Ce_3 (M)		VGA Thermal			
	I2Cf_3 (M)			APU	S5
	I2Cf_1 (M)	Lan	Wlan		S5
	I2Cf_0 (M)	Dimm	Clk Gen		S0



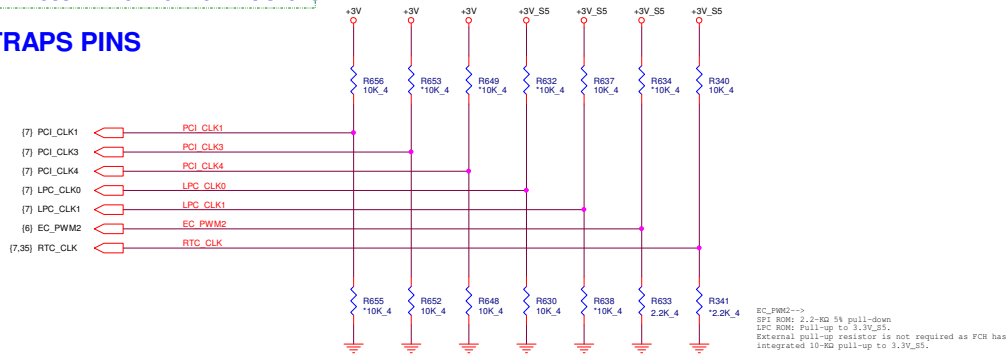






OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

## STRAPS PINS

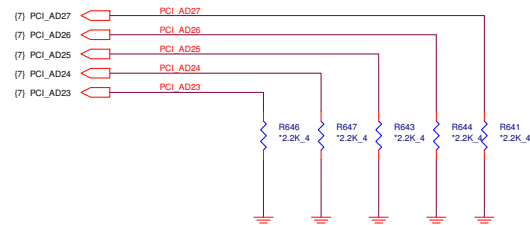


## REQUIRED STRAPS

	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

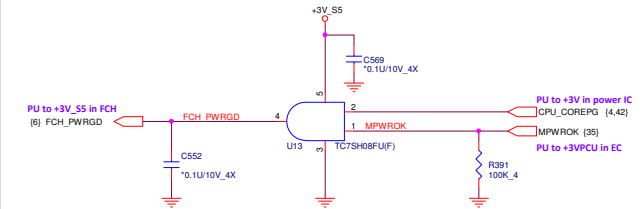
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

## FCH POWER GOOD CIRCUIT



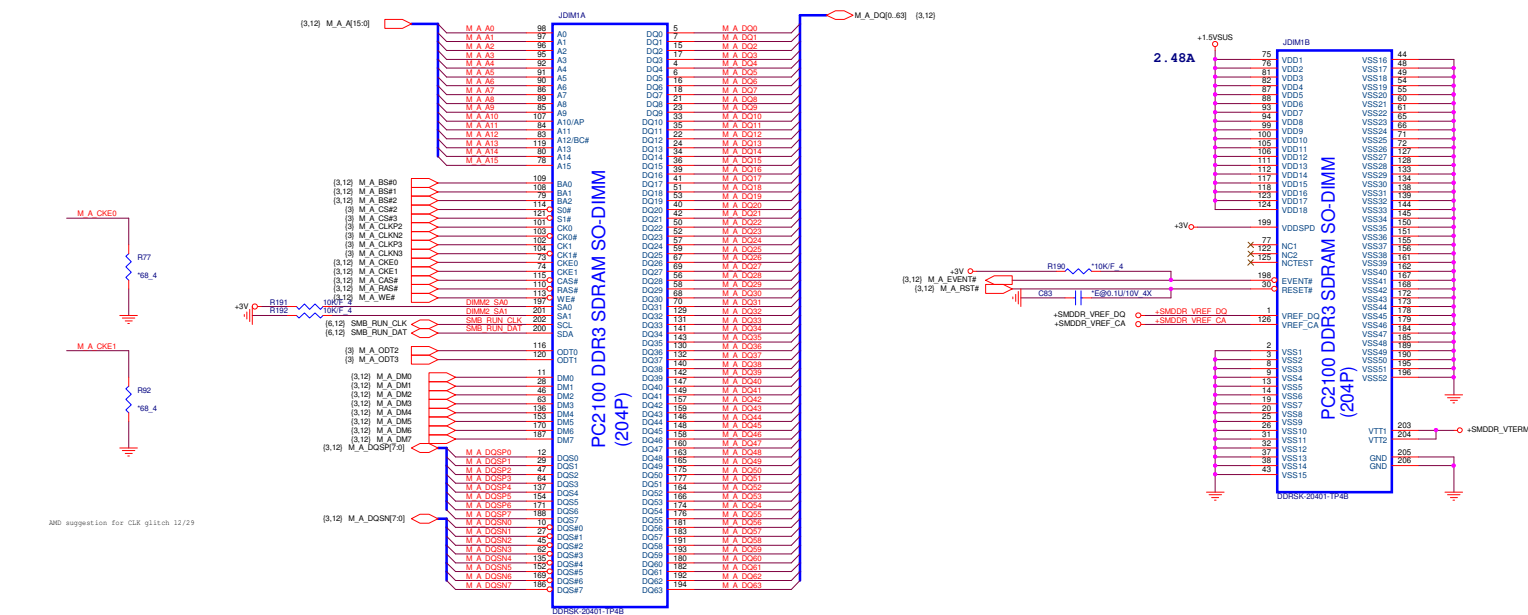
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Quanta Computer Inc.

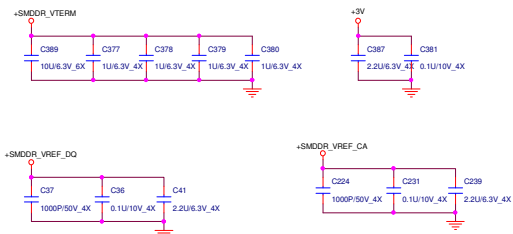
PROJECT : BY7D

Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A
Date	Tuesday, December 11, 2012	Sheet 10 of 46

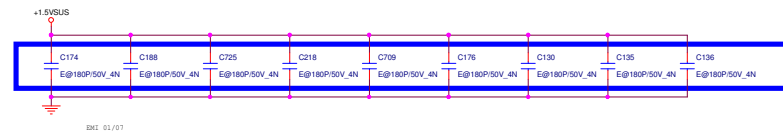
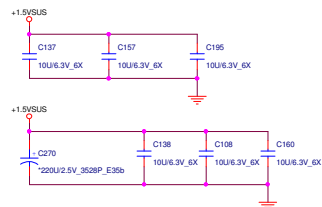


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### TERMINATOR DECOUPLING CAPACITOR



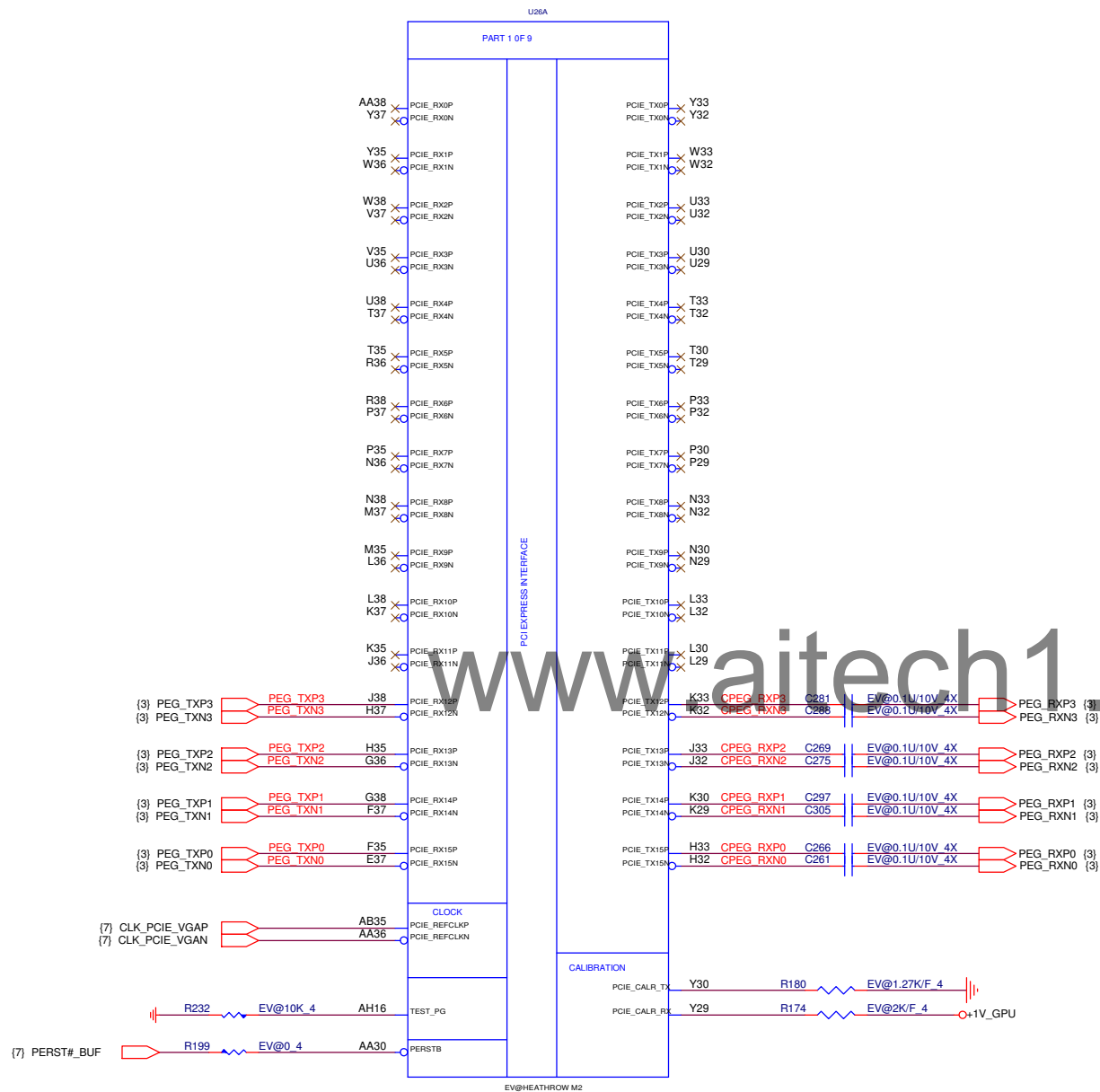
### 9.12A (VCC plane from source)





9.12A (VCC plane from source)



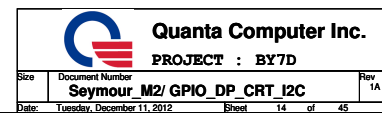


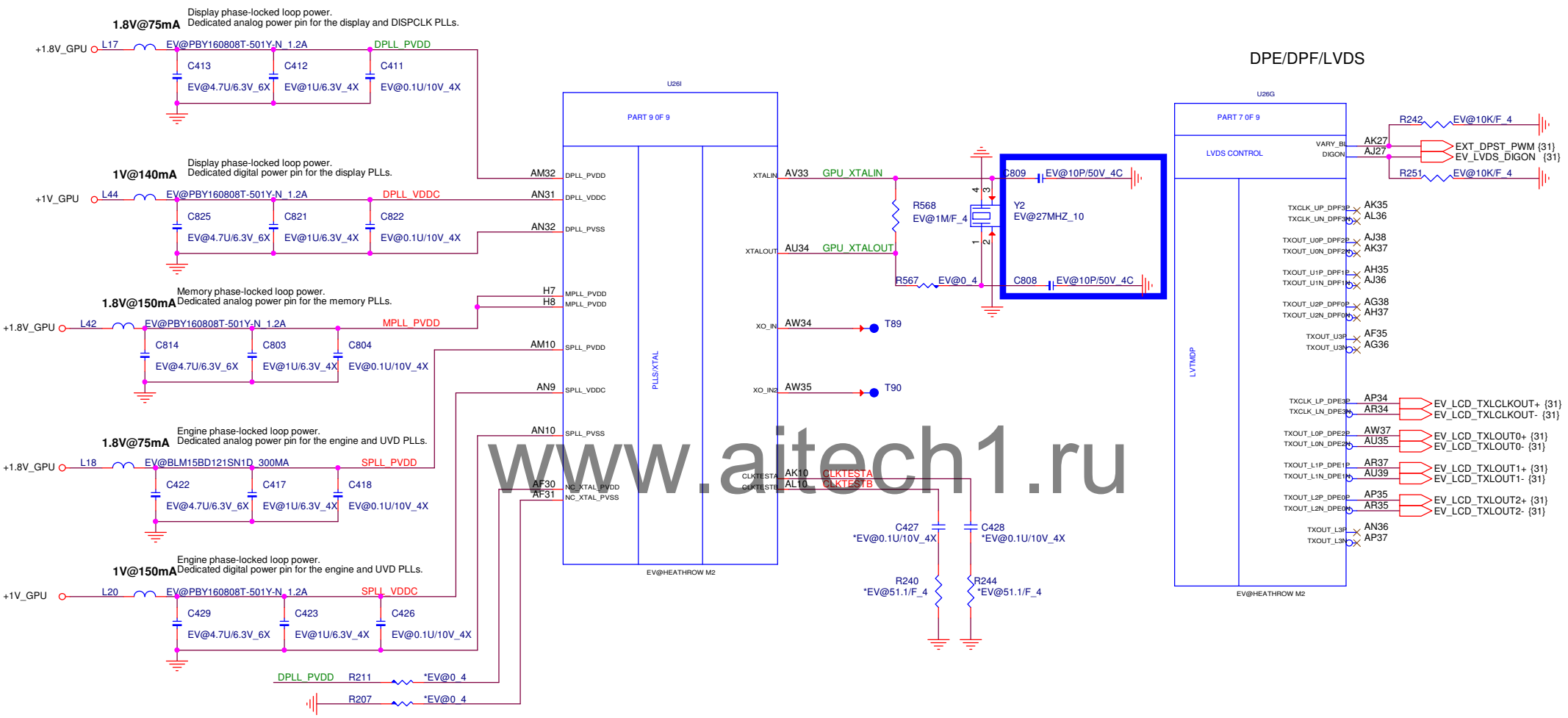
### Seymour Power-on sequence

- 1 => +1V\_GPU
- 2 => +3V\_GPU
- 3 => +VGPU\_CORE,+1.5V\_GPU
- 4 => +1.8V\_GPU

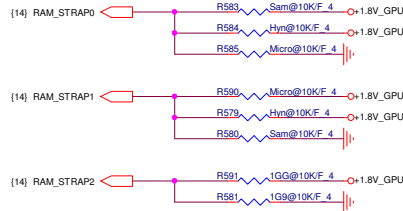
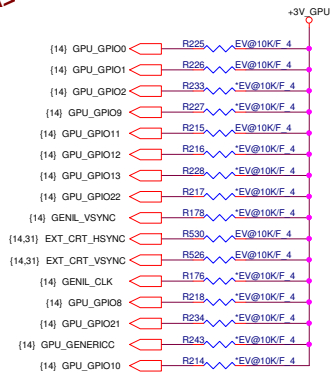
### PEG

Intel platform: Lane0 ~ Lane15  
Brazos platform: Lane12 ~ Lane15  
Comal and Sabine platform: Lane8 ~ Lane15





## &lt;VGA&gt;



## DDR3 Memory TYPE

900/1000 Mhz Vendor

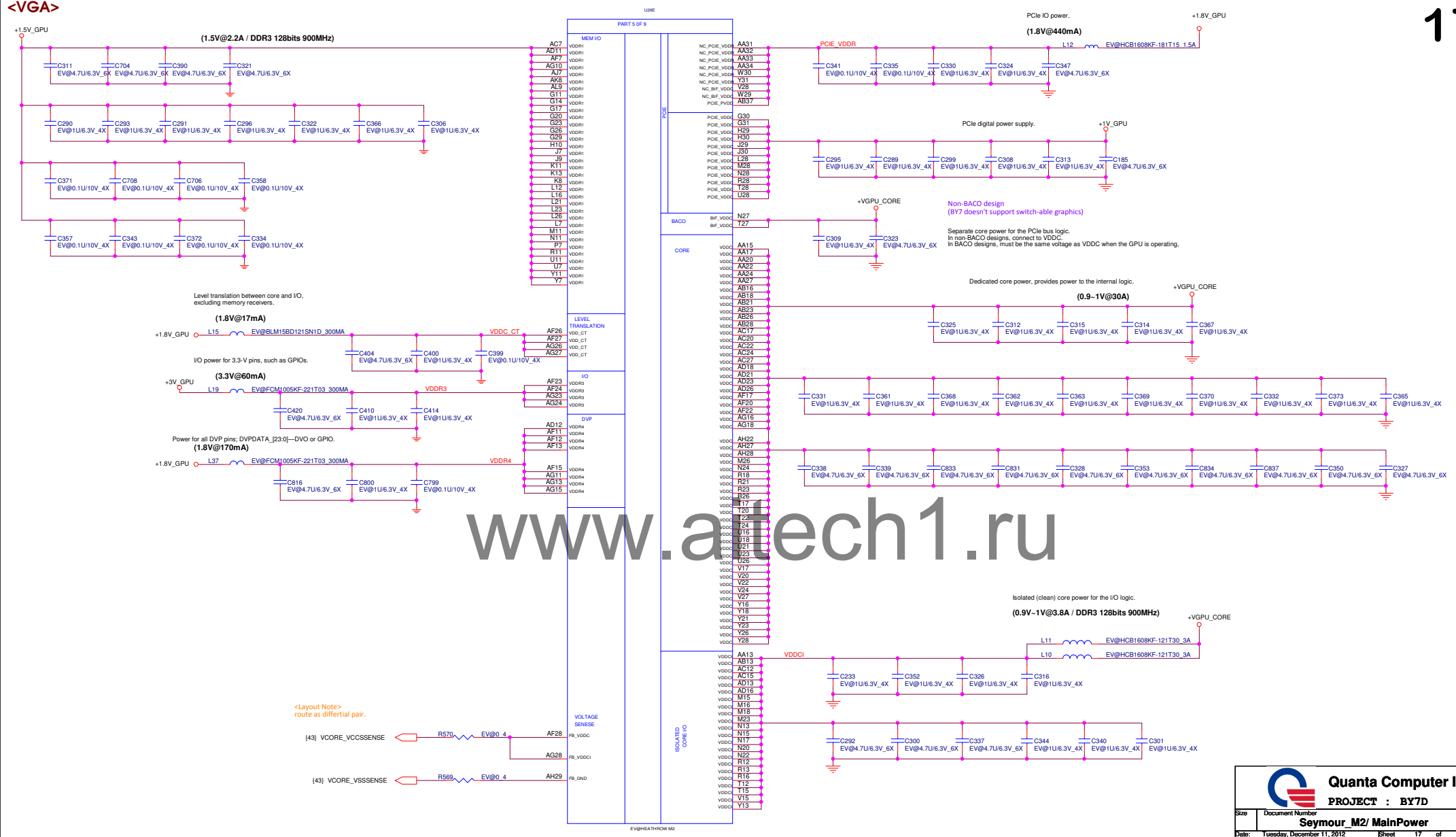
Vendor	Vendor P/N	STN B/S P/N	Frequency	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Samsung	K4W2G1646E-BC11	AKD5MGGT520	900Mhz	1GB	0	0	1
	K4W2G1646E-BC1A	AKD5MGGT532	1000Mhz	1GB	1	0	1
Micro	MT41K128M16JT-107G:K	AKD5DGSTL00	900Mhz	1GB	0	1	0
Hynix	H5TQ2G63DFR-11C	AKD5MGWTW16	900Mhz	1GB	0	1	1
	H5TQ2G63DFR-N0C	AKD5MGDTW01	1000Mhz	1GB	1	1	1

CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select  If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET  Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 5 usable endpoints 000 = all endpoints are usable	XXX

## System Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

## EEPROM



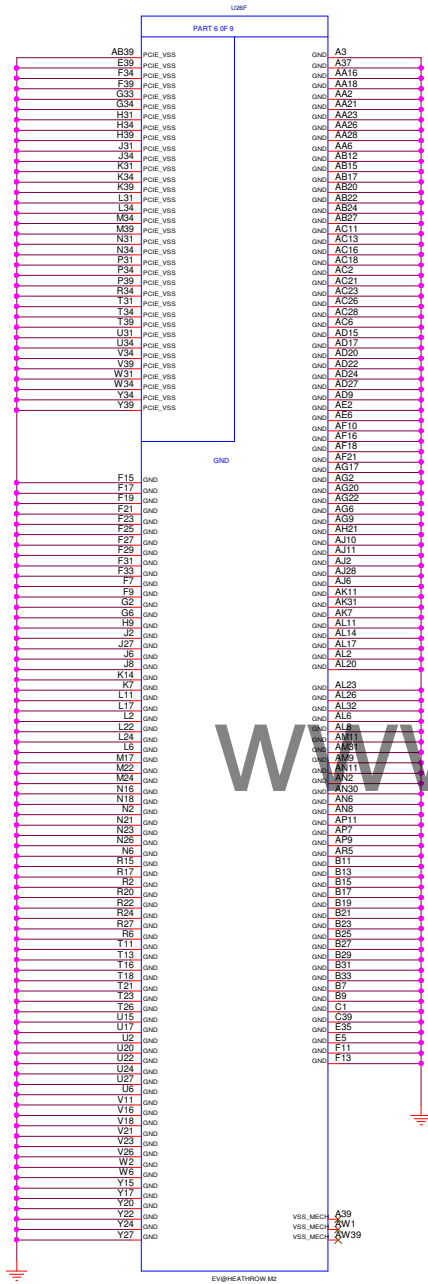
For Thames/Whistler/Seymour  
a dedicated BEAD is required  
for each DPAB VDD10, DPCD VDD10, DPEF VDD10

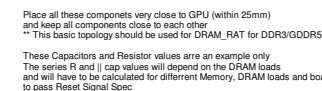
DP/TMDS/LVDS Transmitter Power  
DP mode: 1.8V@188mA per port  
HDMI mode: 1.8V@237mA per port

The schematic diagram illustrates the DP transmitter circuit, organized into several functional blocks:

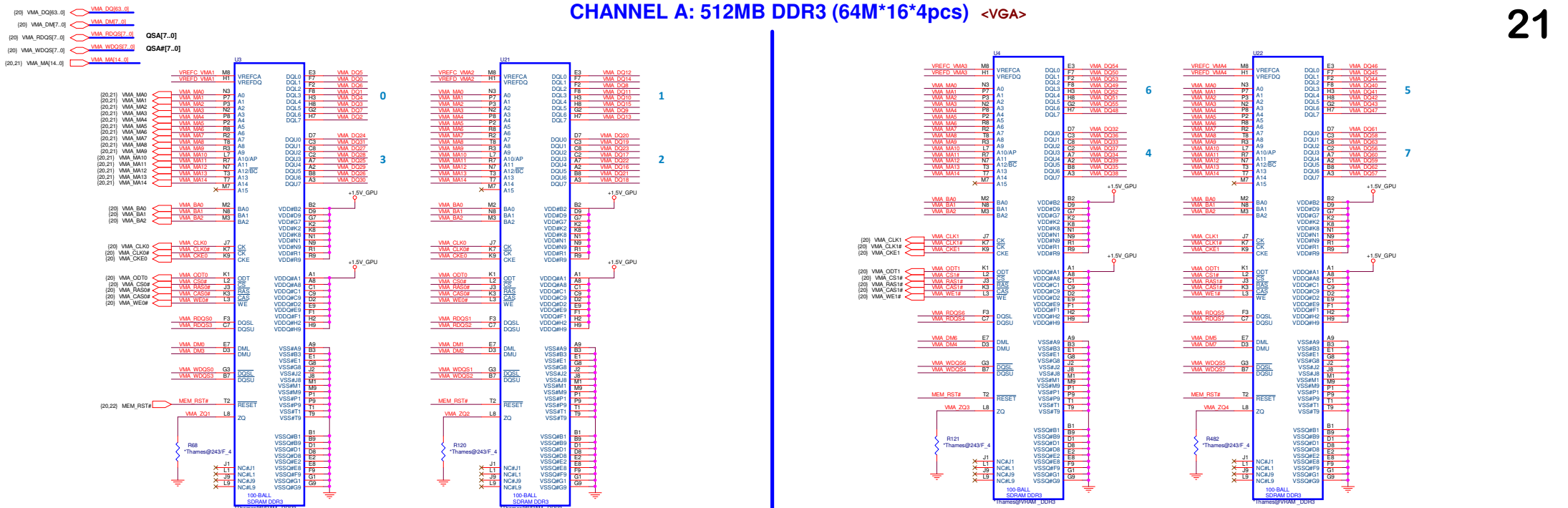
- Power Supply Regulation:**
  - +1.8V\_GPU:** Derived from a +1.8V input through inductor L39, regulated by the DPAB VDD18 module (C811, C796, C806) to provide DP\_VDDP and DP\_VDDR.
  - +1.8V\_GPU:** Derived from a +1.8V input through inductor L38, regulated by the DPCD VDD18 module (C812, C807, C797) to provide DP\_VDDP and DP\_VDDR.
  - +1.8V\_GPU:** Derived from a +1.8V input through inductor L36, regulated by the DPEF VDD18 module (C772, C775, C780) to provide DP\_VDDP and DP\_VDDR.
- Signal Conditioning and Calibration:**
  - AW28, AW18, AM39:** Precision resistors (R578, R576, R552) used for calibration, each with a value of EV@150/F 4.
  - DPAB\_CALR, DPCD\_CALR, DPEF\_CALR:** Calibration points for the DPAB, DPCD, and DPEF modules.
- DP\_VDDP and DP\_VDDR Connections:**
  - DP\_VDDP:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.
  - DP\_VDDR:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.
- DP\_VDDP and DP\_VDDR Connections:**
  - DP\_VDDP:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.
  - DP\_VDDR:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.
- DP\_VDDP and DP\_VDDR Connections:**
  - DP\_VDDP:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.
  - DP\_VDDR:** Connected to various pins including AP26, AU28, AV29, AP20, AP21, AP22, AP23, AU18, AV19, AH34, AJ34, AF34, AG34, AM37, AL38, AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, and AM35.

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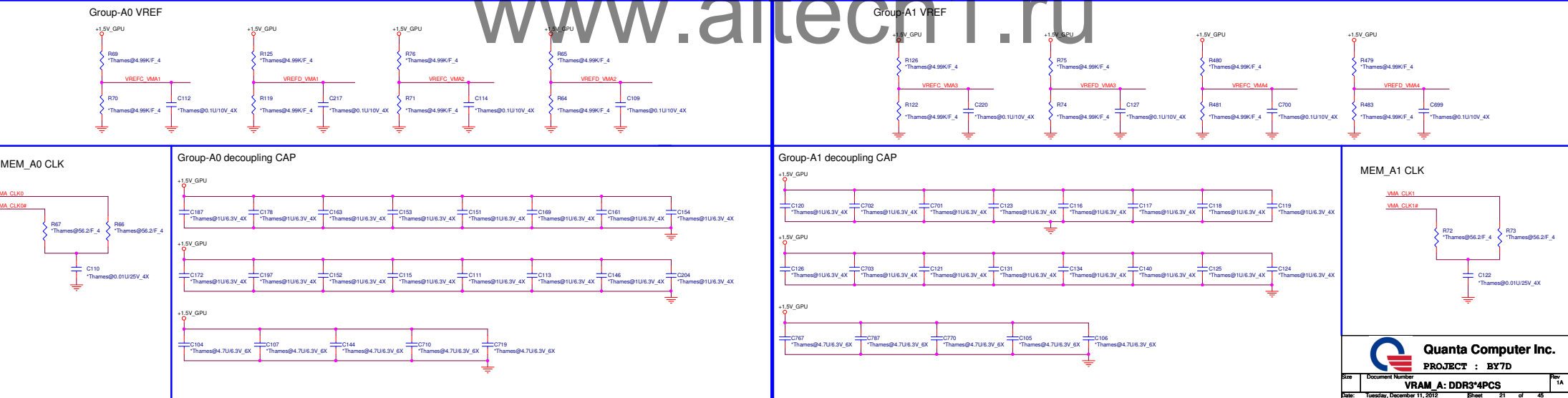




## CHANNEL A: 512MB DDR3 (64M\*16\*4pcs) &lt;VGA&gt;

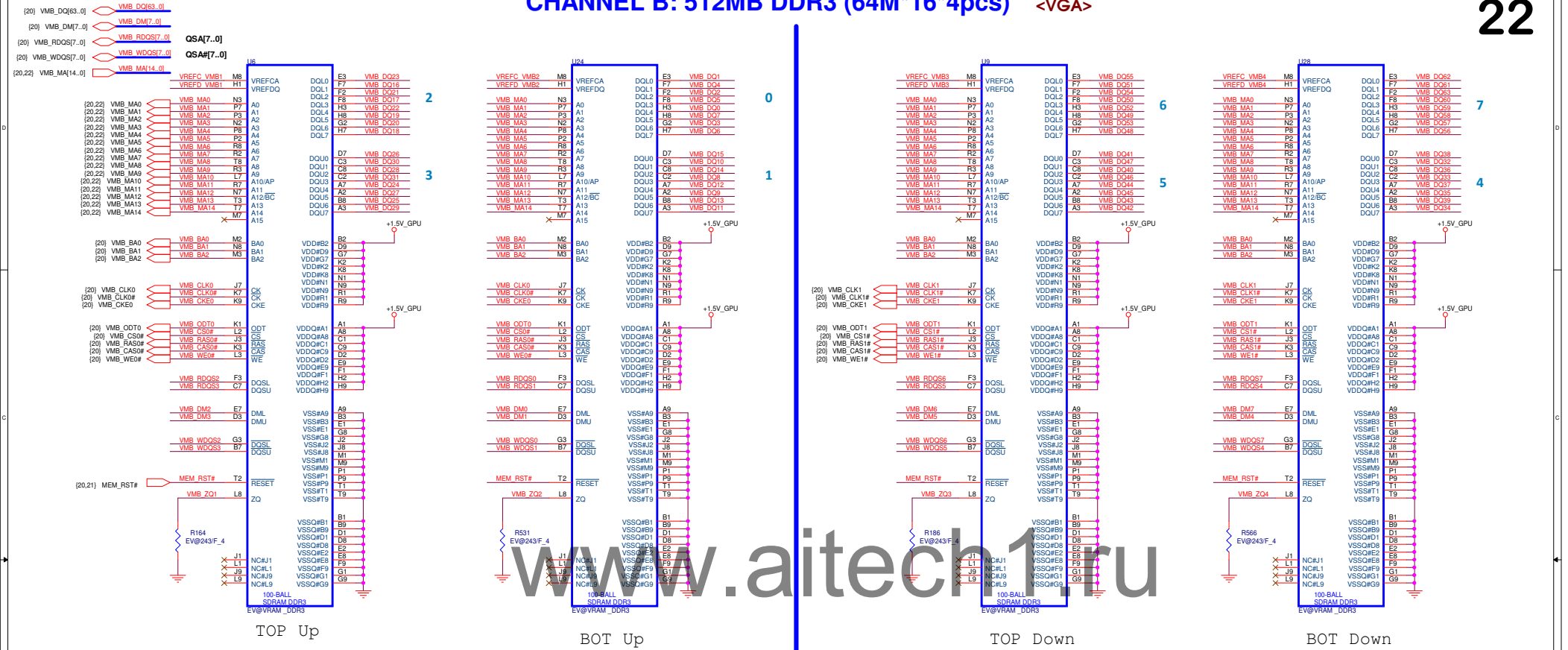


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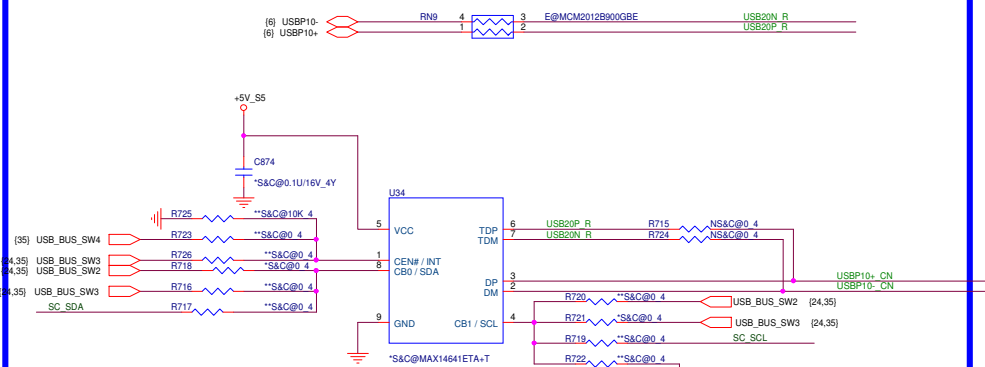
# CHANNEL B: 512MB DDR3 (64M\*16\*4pcs) <VGA>

22



Non-BACO design  
(Brazos doesn't support Muxless Switch-able Graphics)

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	R723	R726	R721	R722	R725	R718	R716	R717	R719
14566		V		V					
14600			V			V			
14617(with CB2)	V		V		V				
14617(no CB2)		V			V				
14641/14642/14644		V			V				
14640							V	V	

SW2	SW3	14600
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	0	Pass-Through (USB) mode
1	1	pass-through (USB) with CDP Emulation

Charger , AM  
Charger , FM  
USB , PM  
USB , CM

SW3	SW2	14641
CB1	CB0	Status
0	0	2A Auto mode for Apple device
1	0	Force 1A for Apple device
0	1	Pass-Through (USB) mode
1	1	pass-through (USB) with CDP Emulation

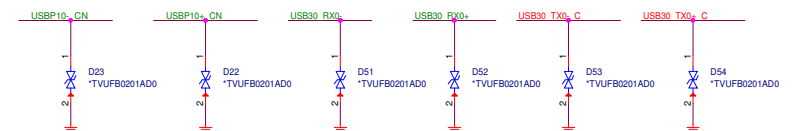
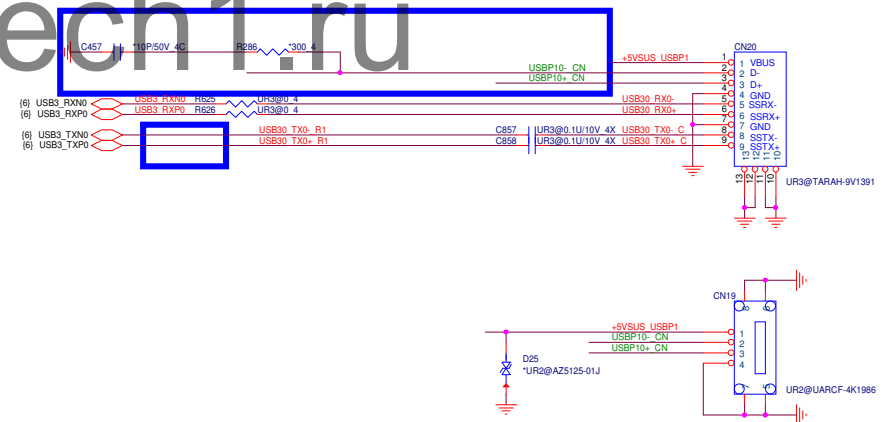
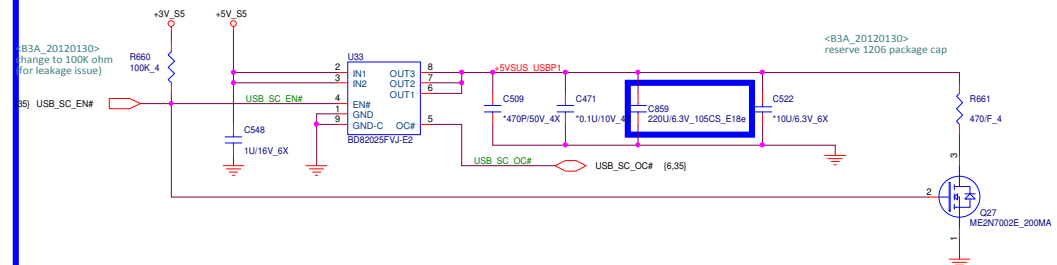
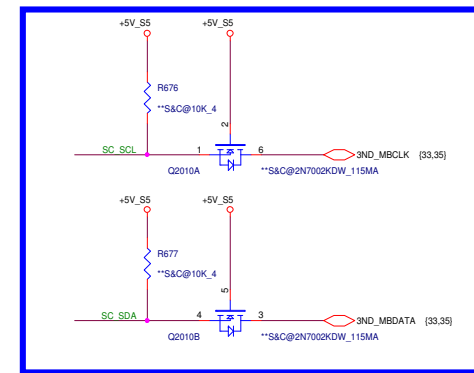
Charger , AM2  
Charger , FM1  
USB , PM  
USB , CM

SW3	SW2	14644
CB1	CB0	Status
0	0	2A Auto mode for Apple device
1	0	Force dedicated charger mode
0	1	Pass-Through (USB) mode
1	1	pass-through (USB) with CDP Emulation

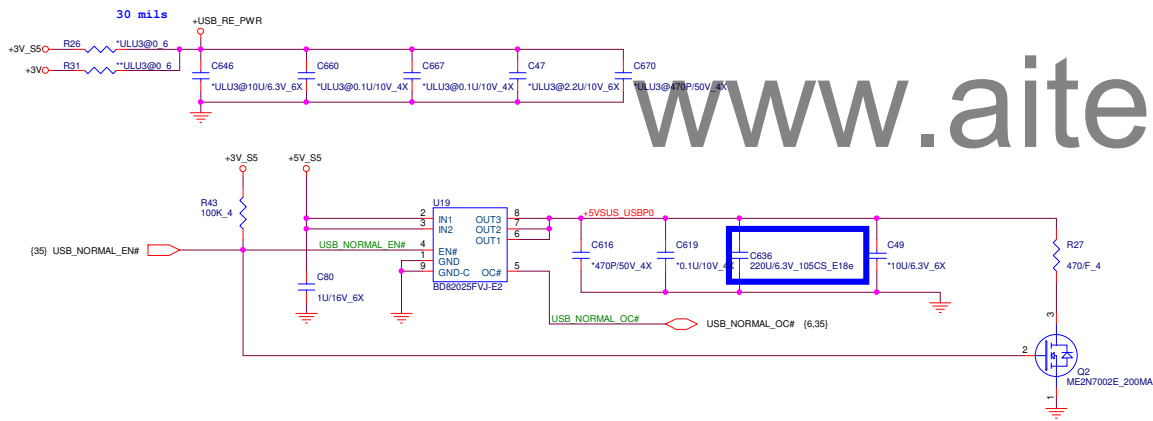
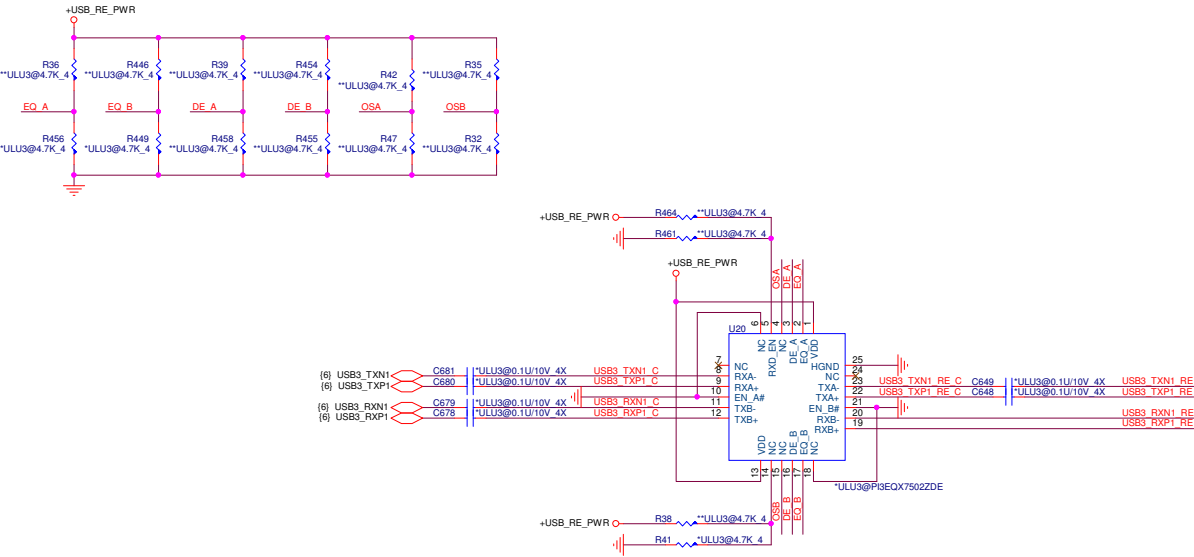
Charger , AM2  
Charger , FM  
USB , PM  
USB , CM

SW3	SW2	14642
CB1	CB0	Status
X	0	2A Auto mode for Apple device
0	1	Pass-Through (USB) mode
1	1	pass-through (USB) with CDP Emulation

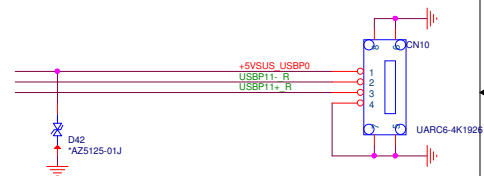
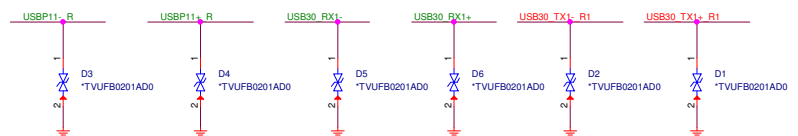
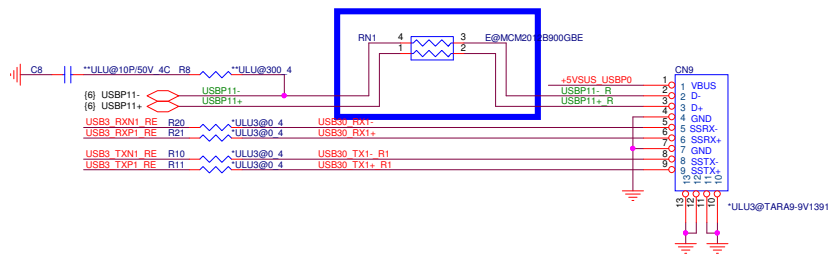
Charger , AM2  
USB , PM  
USB , CM



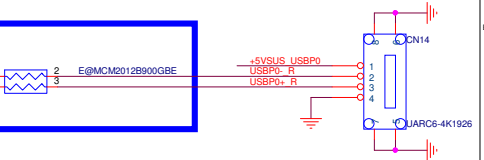
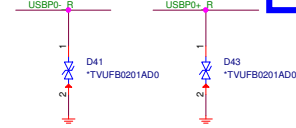
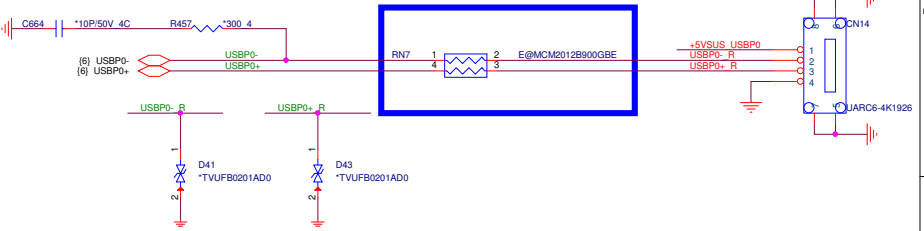
USB 3.0 Power switch



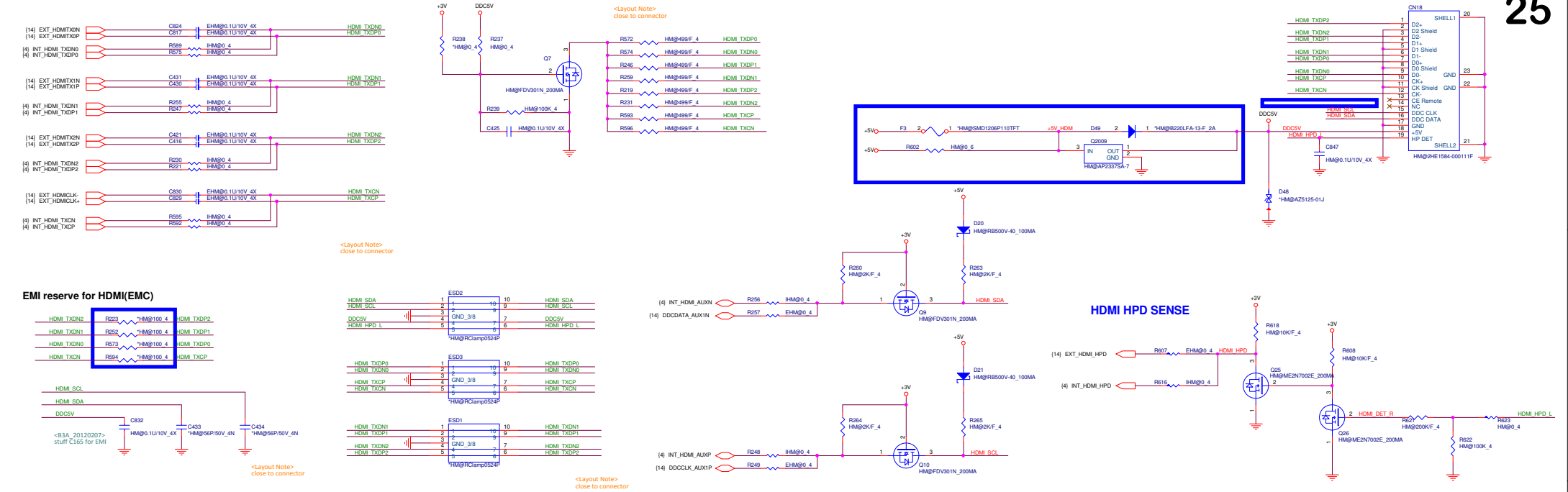
USB CONN LEFT UP



USB 2.0 CONN LEFT DOWN



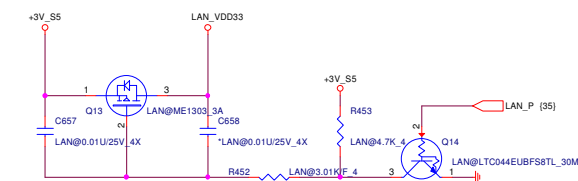
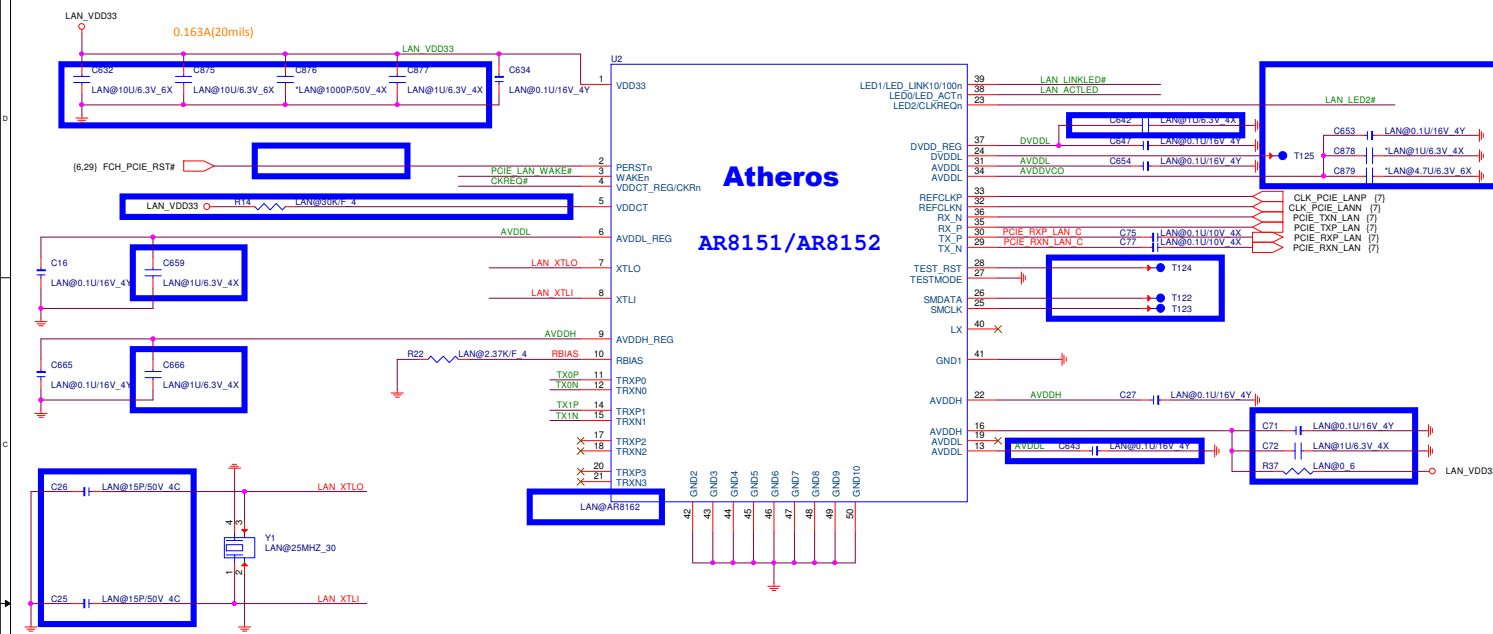
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Remove CEC

## Atheros Lan &lt;LAN&gt; &lt;LNG&gt;

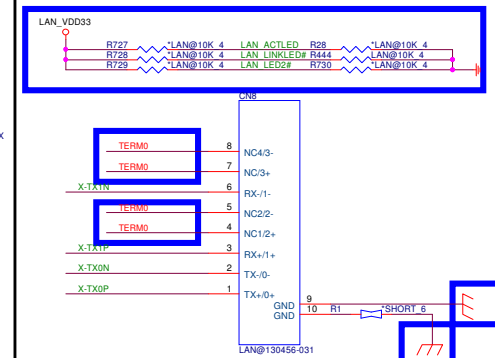
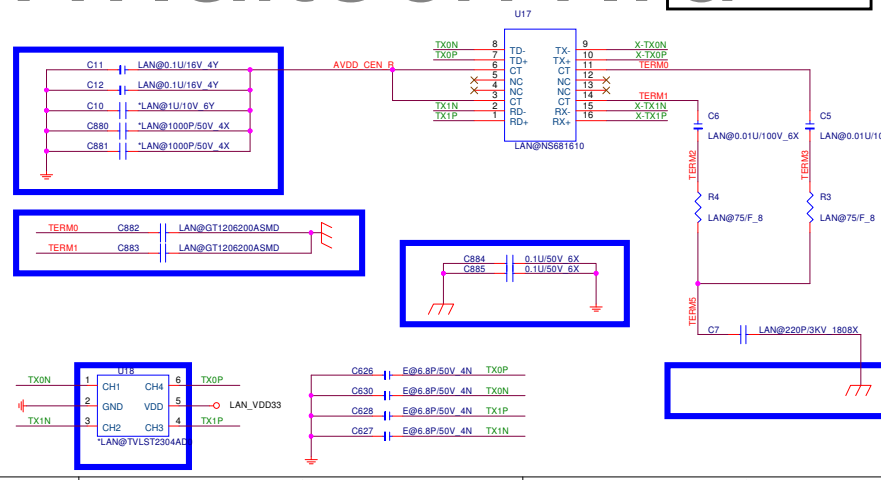
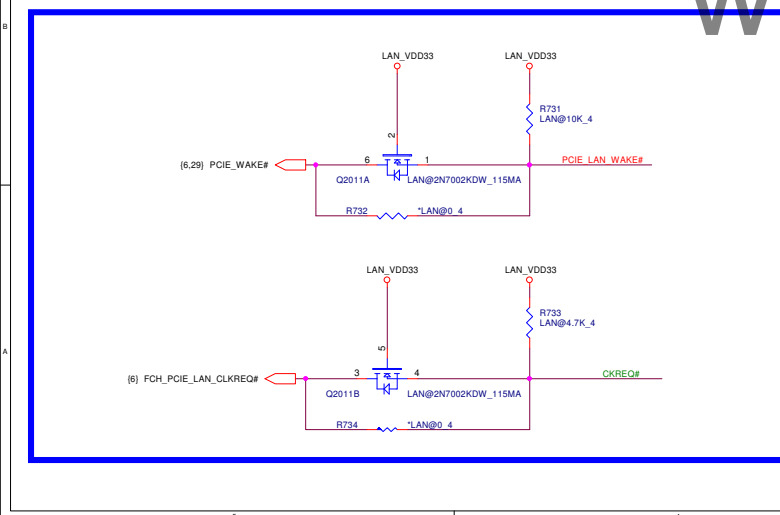


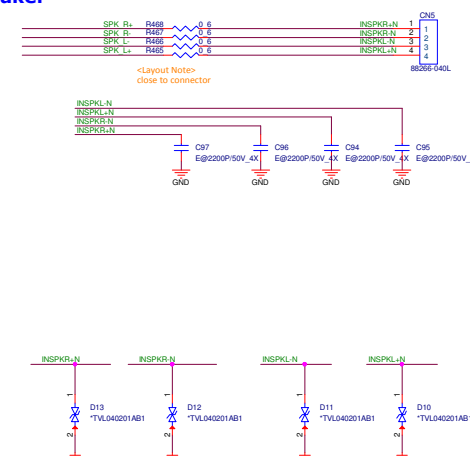
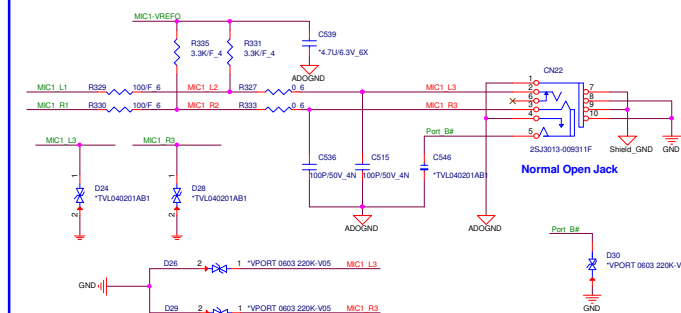
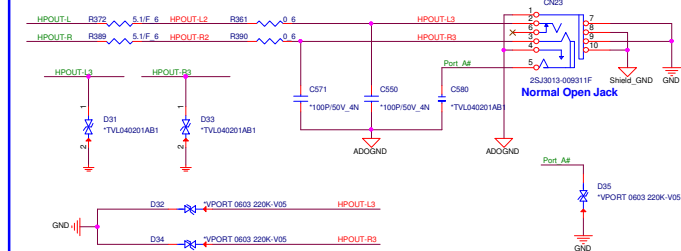
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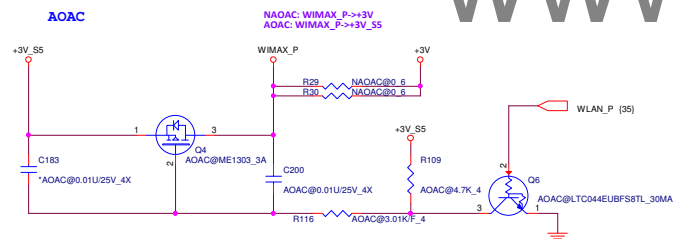
## TRANSFORMER CONN &lt;LAN&gt; &lt;LNG&gt;

10/100:DB0EF7LAN01  
GIGA DB0Z06LAN00

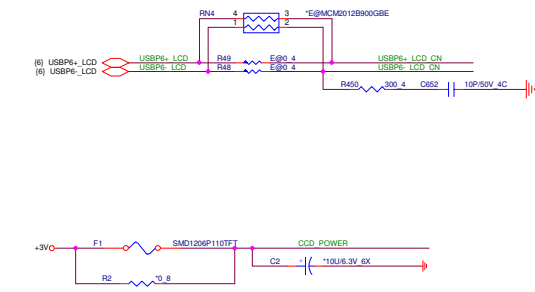
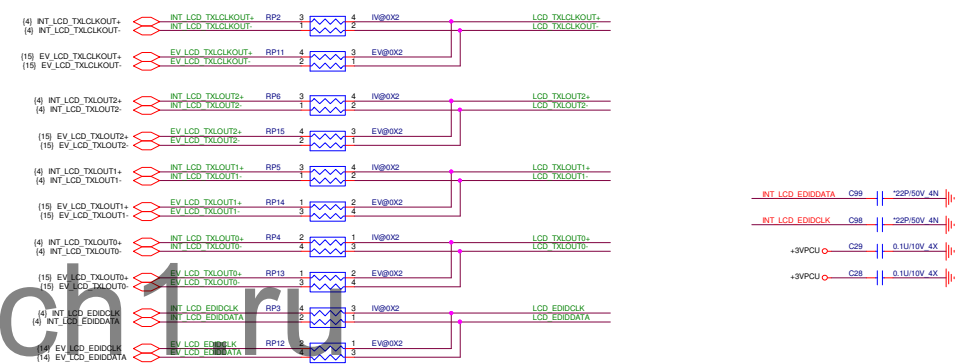
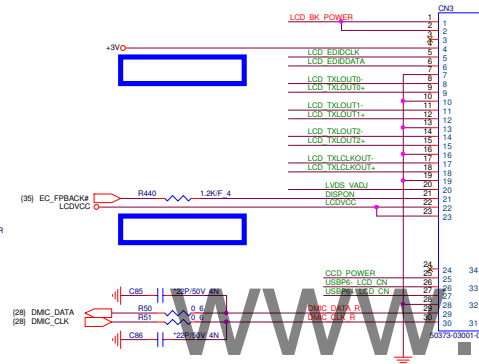
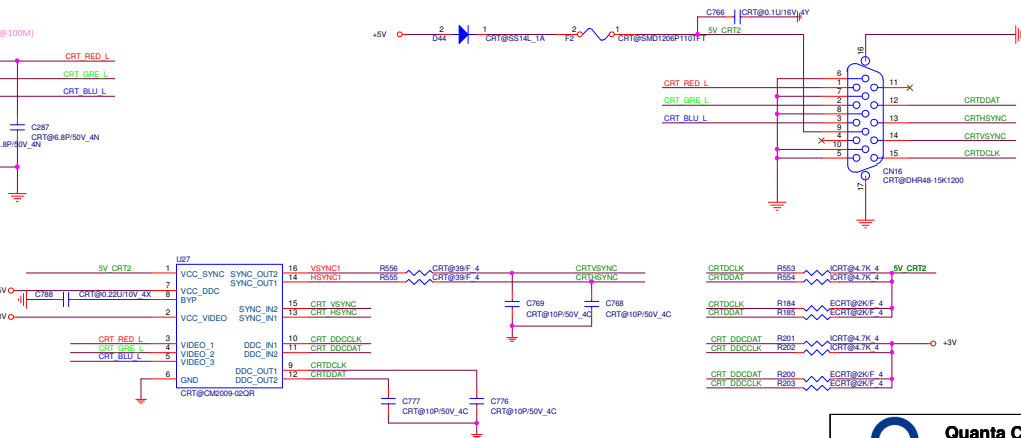
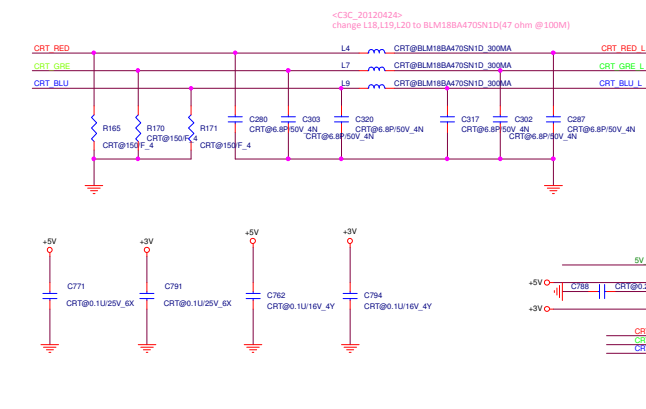
## RJ45 &lt;LAN&gt; &lt;LNG&gt; &lt;LN1&gt;





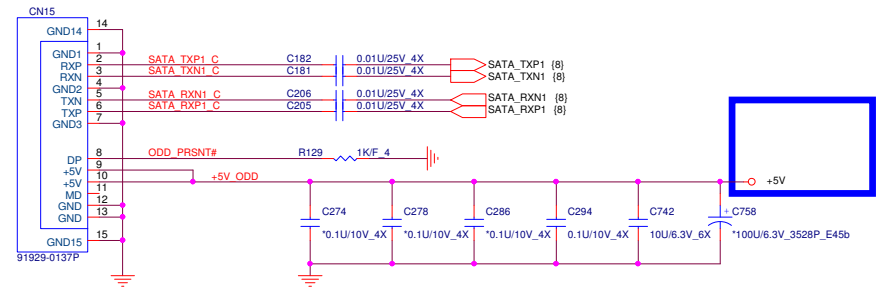




[illegible][illegible][illegible][illegible]

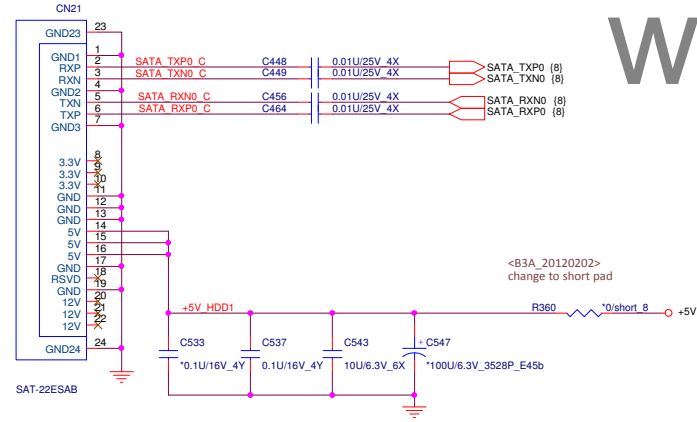
SATA ODD [ODD]

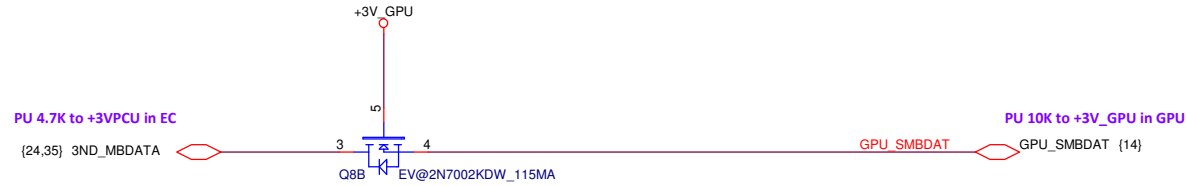
ODD Zero power [OZP]



SATA HDD [HDD]

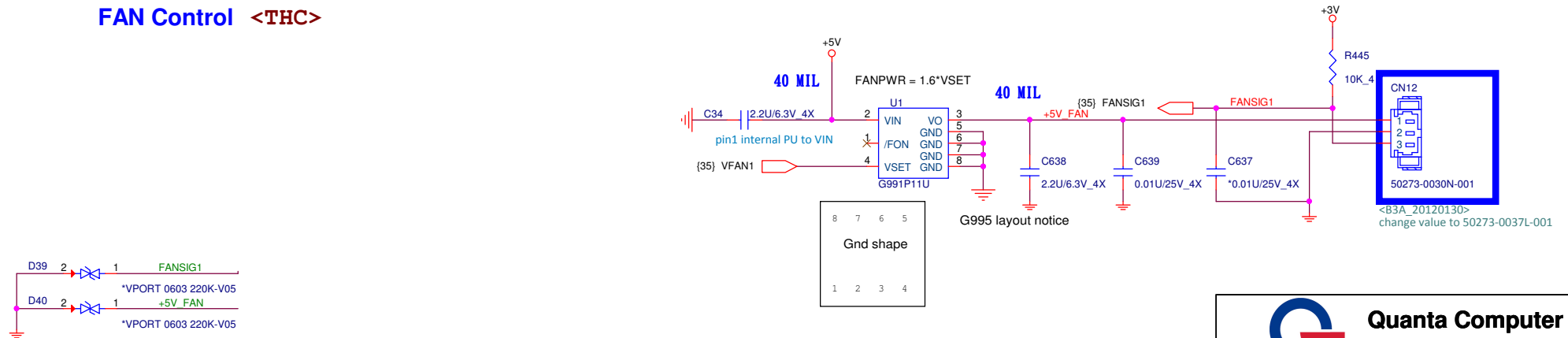
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**FAN Control** <THC>



[illegible]

Schematic diagram of the NBSWON# signal driver circuit. The circuit includes a 2N2222A NPN transistor (Q14031) driven by a PWRLED signal. The transistor's emitter is grounded, and its collector is connected to the NBSWON# signal line through a 0.4 ohm resistor (R17091). The base of the transistor is connected to a PWRLED signal through a 0.4 ohm resistor (R17094). The NBSWON# signal line is also connected to a 5V supply through a 0.4 ohm resistor (R17093) and to a 5VPCU supply through a 0.4 ohm resistor (R17092). The signal line is terminated at the connector (CN2) with a 88513-0401 component.

Schematic diagram of the SMBus interface for the Q2N7002KDW\_115MA component. The diagram shows the SMB\_LAN\_CLK\_Q and SMB\_LAN\_DAT\_Q signals connected to pins 3 and 4 of the component. The SMB\_LAN\_CLK\_Q signal is connected to pin 3, and the SMB\_LAN\_DAT\_Q signal is connected to pin 4. The component is labeled Q2N7002KDW\_115MA. The diagram also shows the internal structure of the component, including the SMB\_LAN\_CLK\_Q and SMB\_LAN\_DAT\_Q signals, and the SMB\_LAN\_CLK\_Q and SMB\_LAN\_DAT\_Q signals. The component is connected to a 3V supply through resistors R736 and R738, both labeled 4.7K\_4.

Pin	Signal
1	+5V0, TPCLK_L
2	TPDATA_L
3	BOARD_ID10
4	+3V0, SMB_LAN_DAT_O
5	SMB_LAN_CLK_O
6	
7	
8	

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HOLE1 HOLE18 HOLE21 HOLE27

\*H-C276BC217D146P2 \*H-C276BC217D146P2 \*H-C276BC217D146P2 \*H-c315bc273d118p2 \*h-tc315bc273d118p2 \*h-c276d118p2

HOLE19 HOLE14 HOLE25 HOLE26 HOLE24

\*H-C256D146PT \*H-C256D146PT \*H-C236D161PB \*h-c236d236n \*H-TC236D161PB

<B3A\_20120130>  
change value to H-C256D146PT

<B3A\_20120130>  
change value to H-TC236D161PB

HOLE5 HOLE23 HOLE3

\*H-C91D91N \*H-C91D91N \*H-C91D91N

HOLE12 HOLE11

\*h-gtbsd118p2 \*H-C256D256N

HOLE22 HOLE21 HOLE17 HOLE4 HOLE18

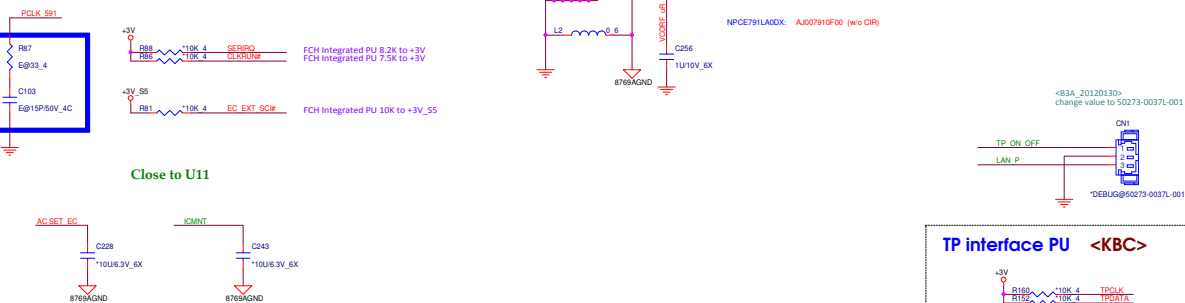
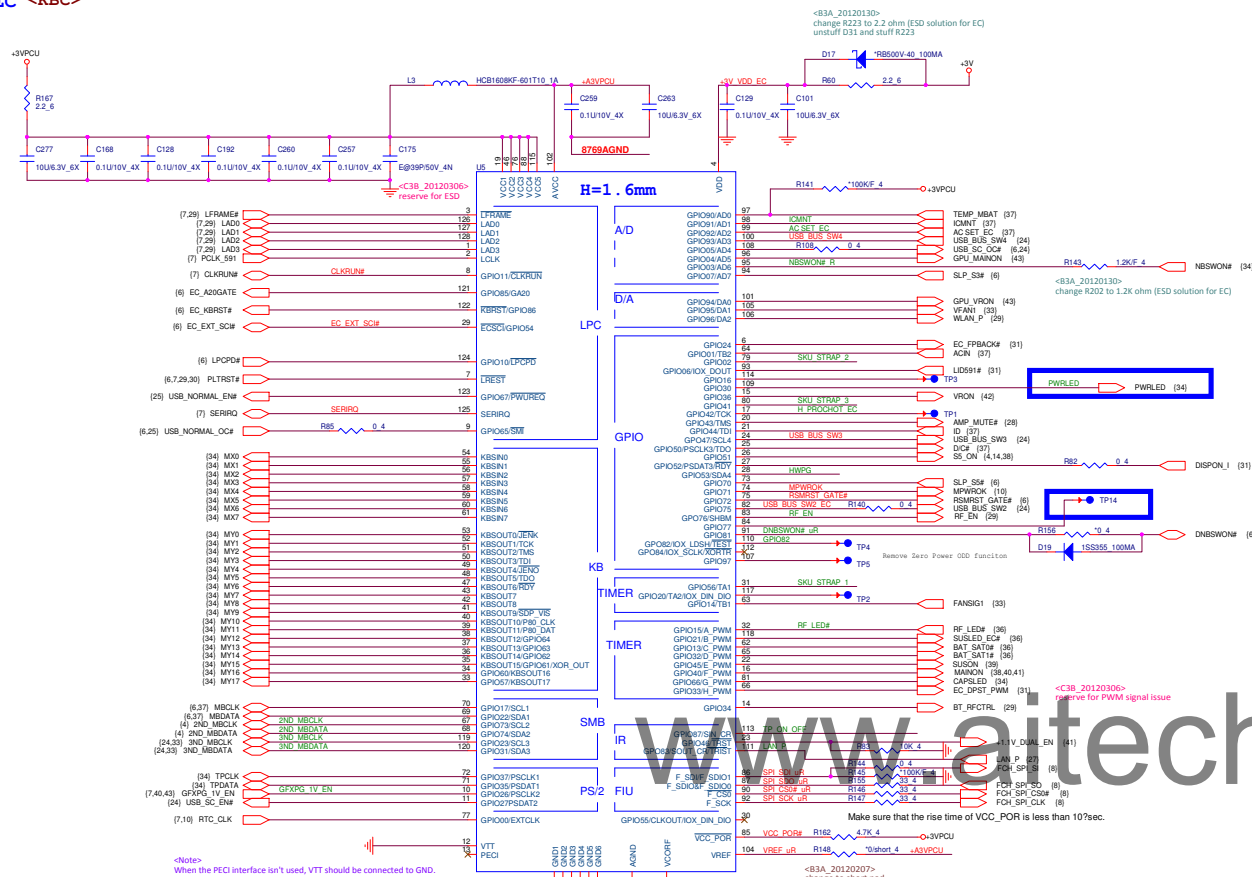
\*hg-c273d118p2 \*hg-c273d118p2 \*HG-C276D118P2 \*HG-C276D118P2 \*HG-C276D118P2

HOLE8 HOLE2 HOLE13 HOLE15

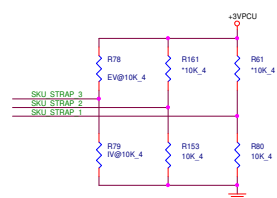
\*O-BY-7 \*H-C236D118P2 \*H-TC197BC131D91P2 \*H-TC197BC131D91P2

Quanta Computer Inc.  
PROJECT : BY7D

Size	Document Number	Project	Sheet	of	Rev
	KBC/TP/FP CONN.				1A
Date:	Tuesday, December 11, 2012		34	of	45



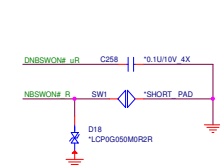
SKU_STRAP_1 (GP1056)	SKU_STRAP_2 (GP1002)	SKU_STRAP_3 (GP1041)	SKU
0	0	0	Brazos UMA
0	0	1	Brazos DIS
0	1	0	COMAL UMA
0	1	1	COMAL DIS
1	0	0	Deccan UMA
1	0	1	Deccan DIS



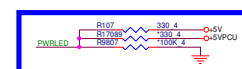
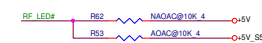
## TP interface PU &lt;KBC&gt;



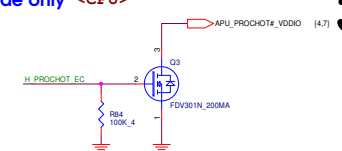
Power Button <KBC>



## LED PU/PD &lt;LED&gt;



Intel Turbo mode only <CPU>



## SM BUS PU &lt;KBC&gt;

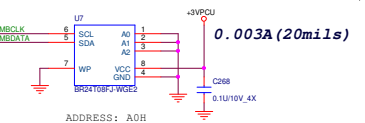
### SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SMLT	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

## Strap &lt;KBC&gt; SHBM



## ID EEPROM &lt;KBC&gt;



## SPI FLASH &lt;KBC&gt;

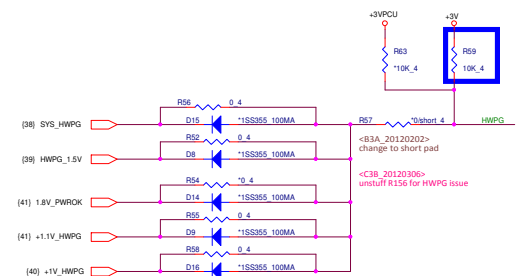
BY6-A1A Del SPI ROM

MX25L3205DM2I-12G: AKE39FP0Z00  
W25Q16BVSSIG: AKE38FP0N01

### INTERNAL KEYBOARD STRIP SET

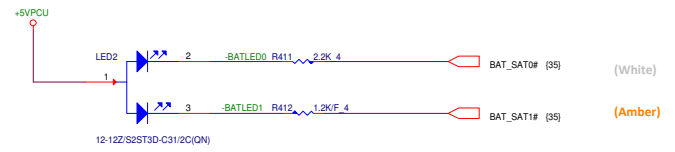


HWPG circuit <KBC>

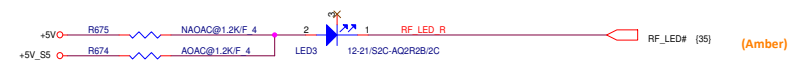


LED <LED>

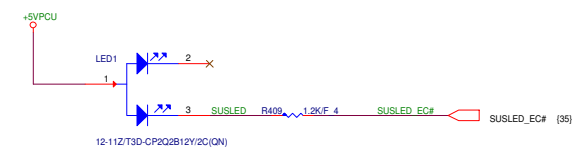
BATTERY



RF LED <LED>

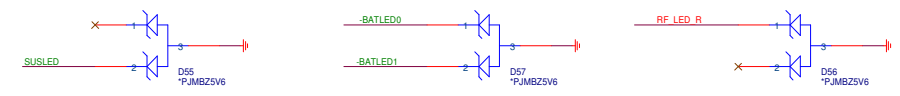


POWER <LED>



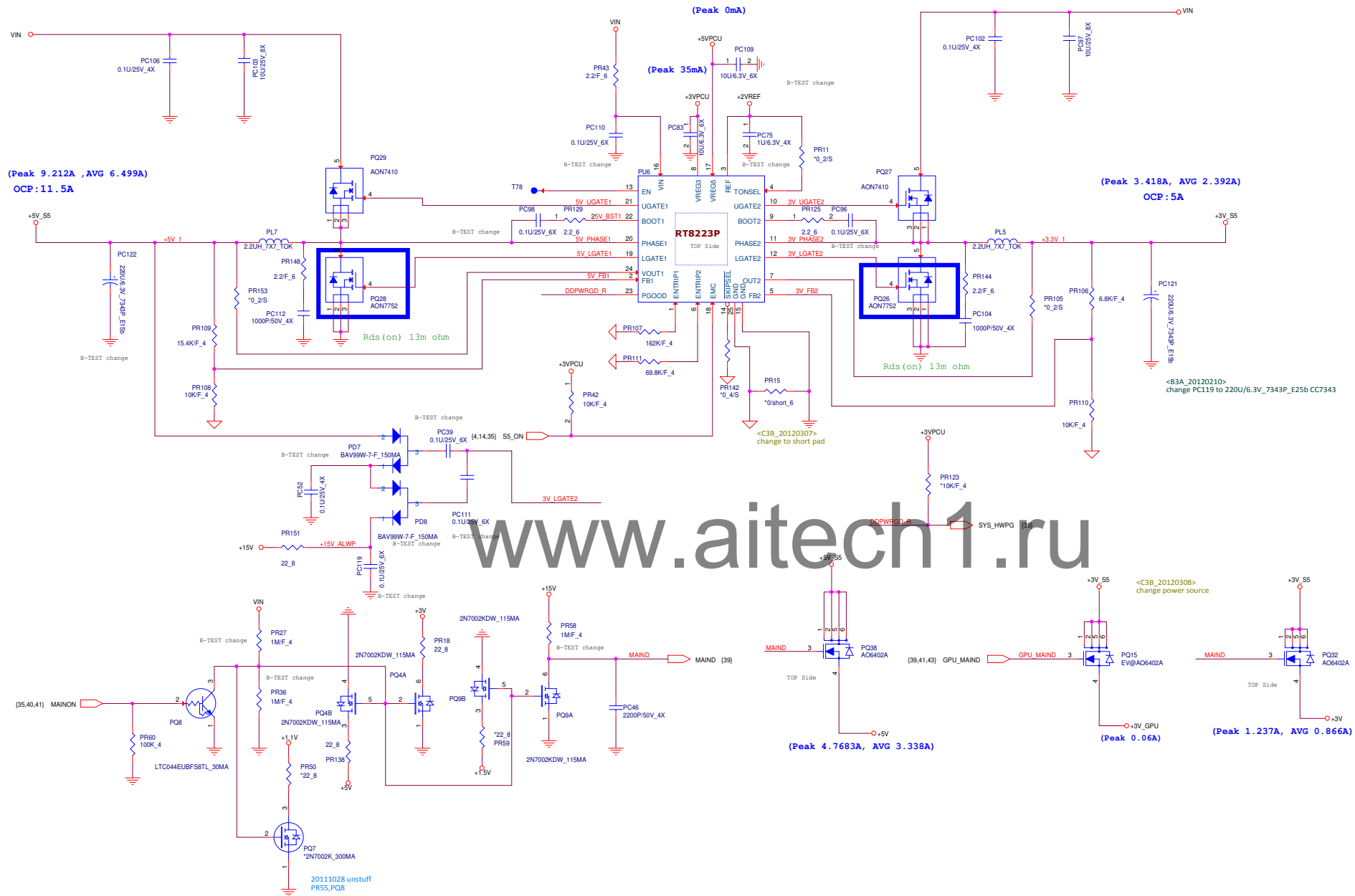
LED P/N	Behavior	res
BEWY0007ZA0 (White/Amber)	power on: White LED bright sleep: Amber LED blink	R135: stuff 1.5K R137: stuff 1.2K
BEWH0051Z00 (White)	power on: White LED bright sleep: White LED blink	R135: unstuff R137: stuff 1.5K

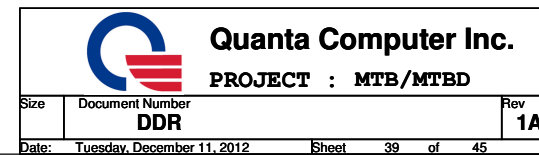
ESD Protect <ESD>

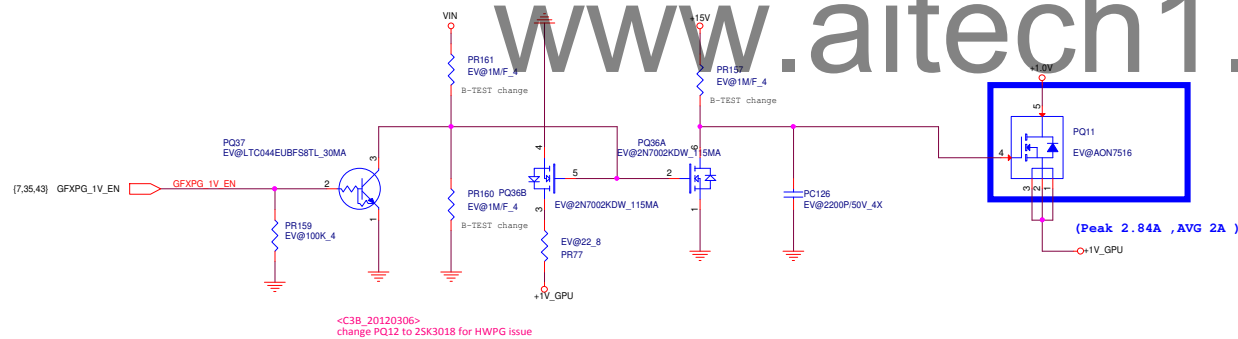
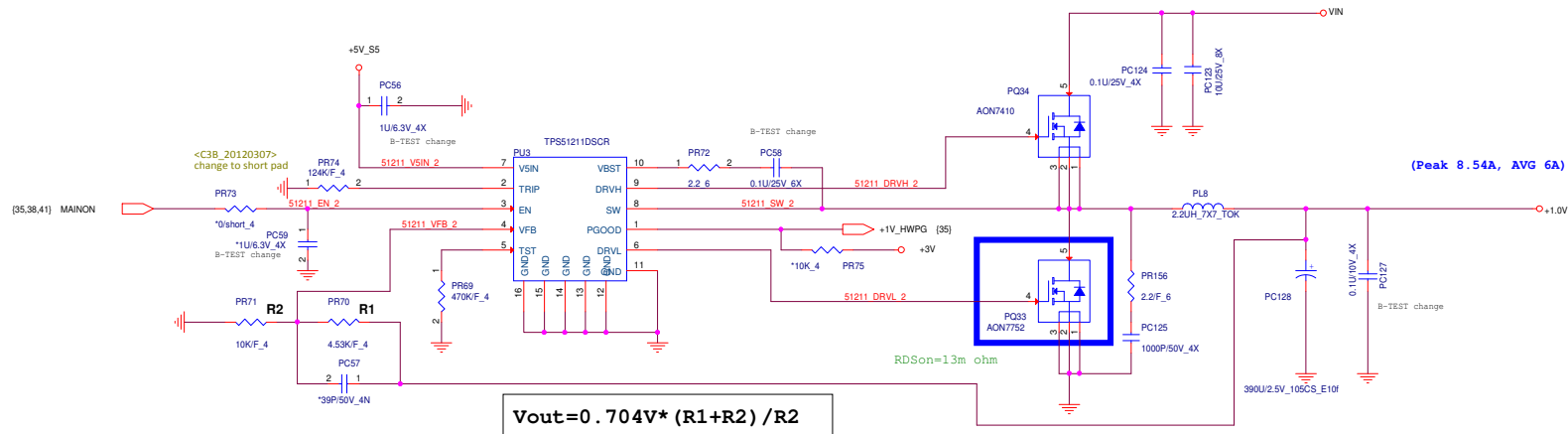


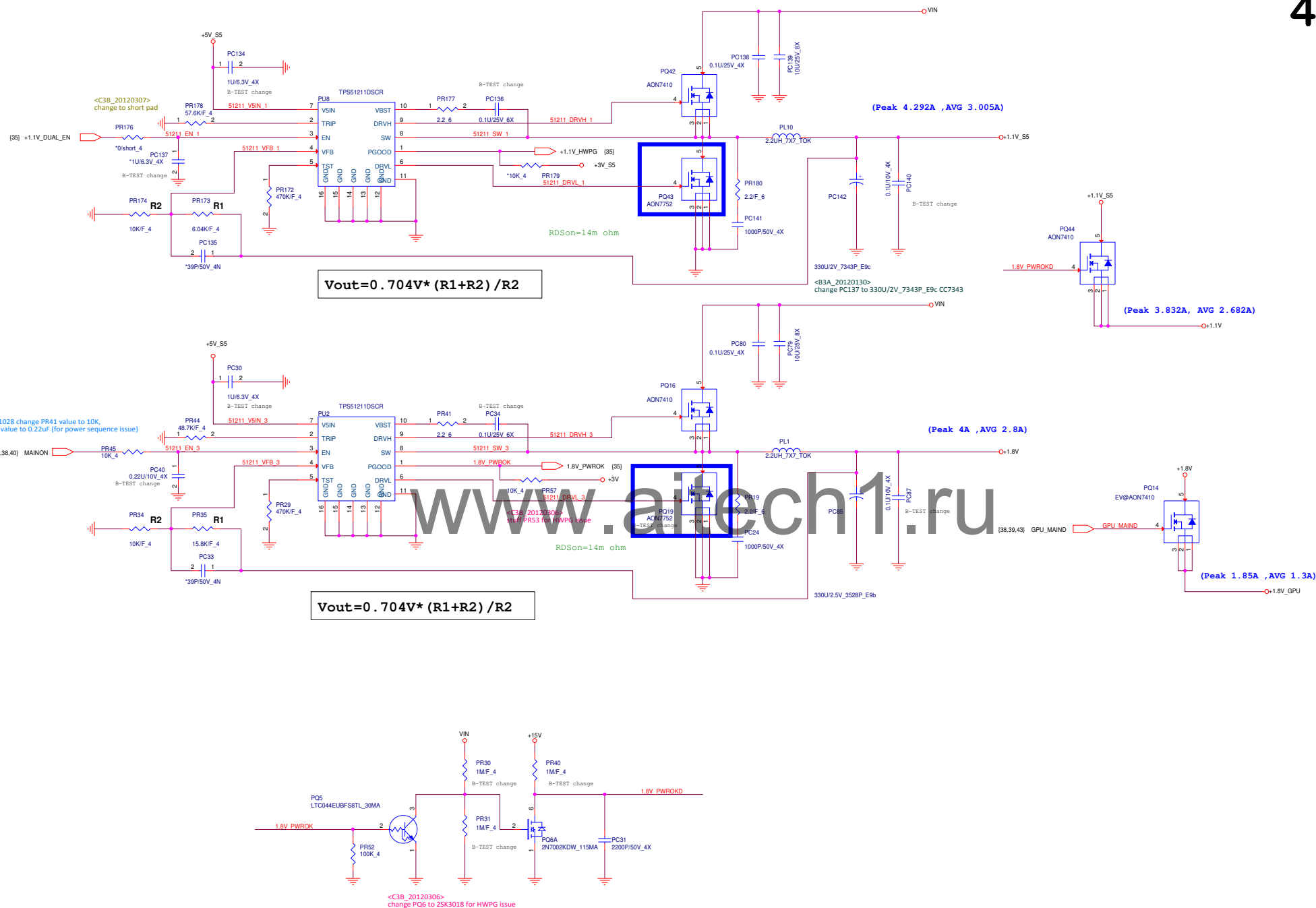
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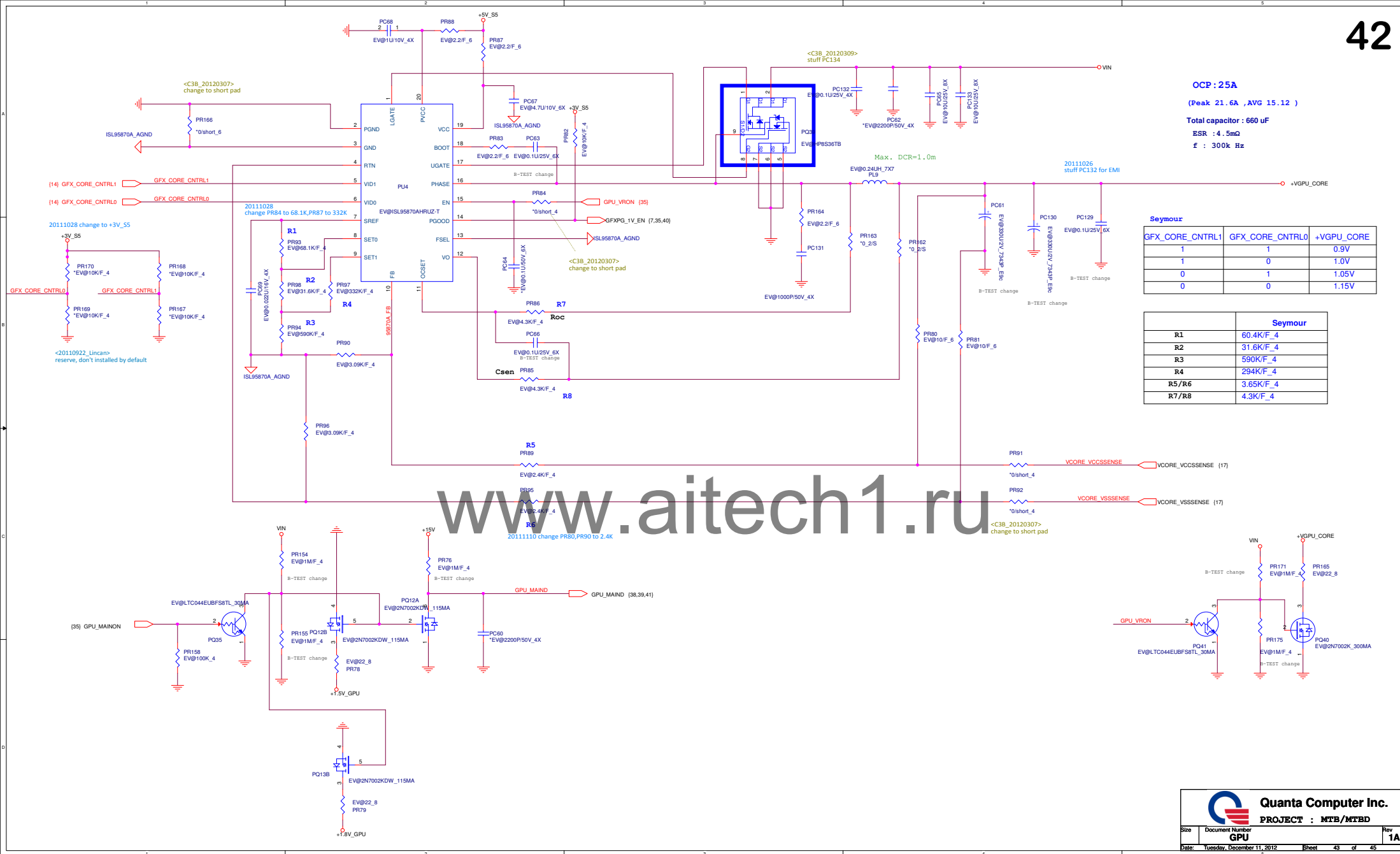




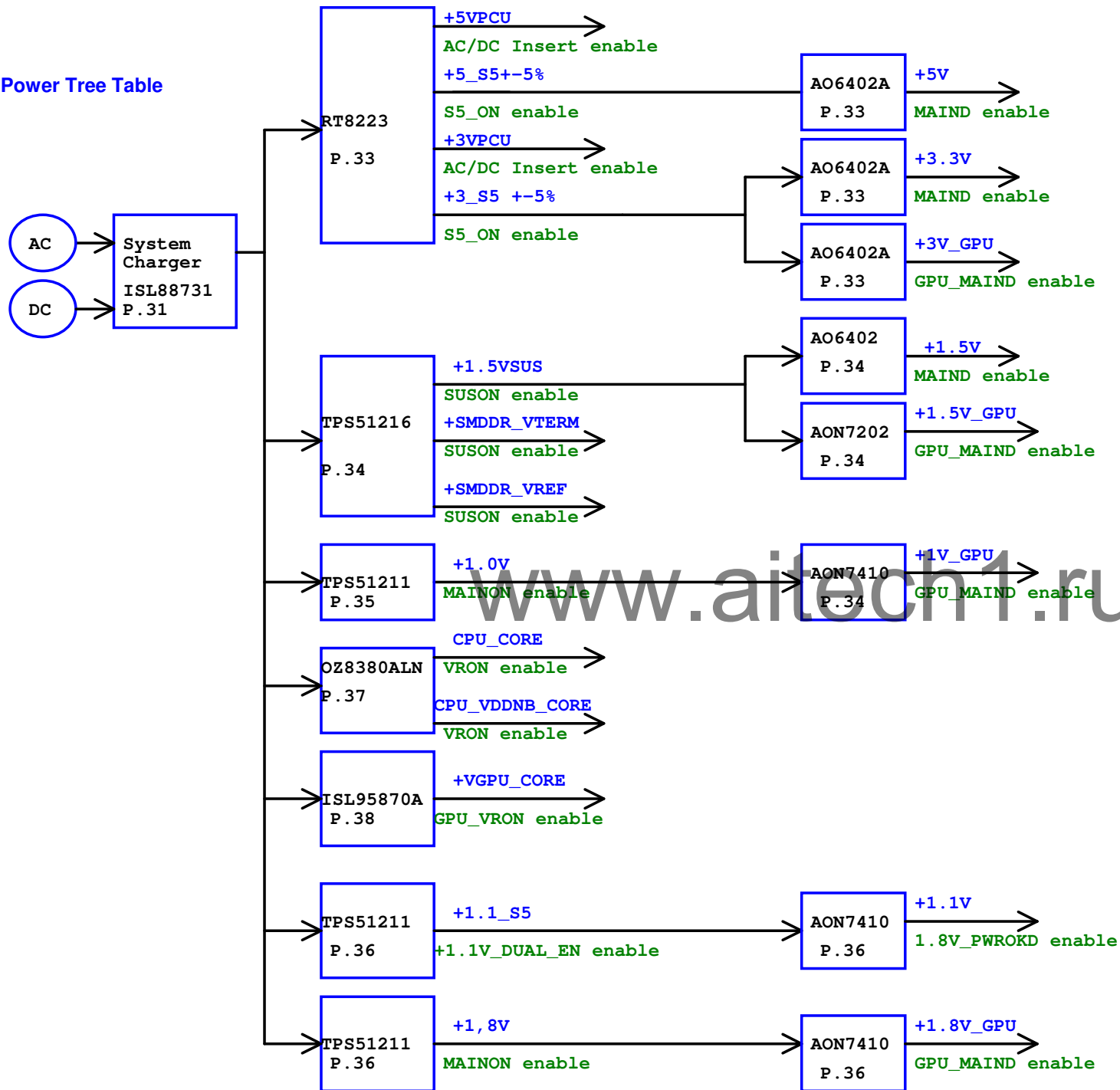








Power Tree Table



[illegible]